International Journal of AI, BigData, Computational and Management Studies
Noble Scholar Research Group | Volume 6, Issue 1, 52-62, 2025
ISSN: 3050-9416 | https://doi.org/10.63282/3050-9416/IJAIBDCMS-V6I1P106

Original Article

Multi-Domain IVRs for Chiplet-Based Processors: Towards Energy-Efficient Power Delivery

Shivakumar Udkar
Senior Manager Design Engineering AMD Inc., Colorado(USA).

Received On: 02/02/2025 ***Revised On: 22/02/2025*** ***Accepted On: 28/02/2025*** ***Published On: 08/03/2025***

Abstract: *The use of advanced processors in the contemporary world results in the implementation of the chiplet architectural design for better scalability, higher performance, and relatively affordable prices. However, power delivery is still problematic in such architectures because interconnects consume more power, the power distribution is non-uniform and this architecture has high power density. Coping with these challenges, the present paper aims to describe the design and implementation of the multi-domain integrated voltage regulators (IVRs) concerning chiplet-based processors with an emphasis on the aspects of energy-saving power delivery. Introducing a new multi-domain IVR which regulates the voltage across chiplets both for getting the better performance of the system and for reducing its power consumption. In order to optimize conversion efficiency and maintain thermal stability, our design adopts DVS, load awareness and adaptive feedback mechanisms. Other than that the conventional mono-voltage regulators, our methods provide discrete control of voltage over many domains leading to lower power wastage in the system.*

To confirm the effectiveness of our strategy, we perform realistic and experimental results using standard processor benchmarks. The outcomes show that the adopted IVR architecture can increase the power conversion efficiency by up to 20% and decrease thermal hotspots by 15% as compared to traditional power delivery methods. Furthermore, the proposed adaptive power management approaches results in turning off voltage droops and improvements in load voltage balancing, so that the total computational throughout increases by 10%. From these results, it is clear that the application of multi-domain IVRs open to opportunities in managing power in chiplet-based processors for the development of subsequent generation energy-dependent computing systems.

Keywords: *Relevant technical terms, Multi-Domain IVRs, Chiplet-Based Processors, Power Delivery, Energy Efficiency, On-Chip Voltage Regulators.*

1. Introduction

1.1. Background and Motivation for Multi-Domain IVRs in Chiplet-Based Processors

Concerning the rapid increase in the SoC complexity, the need for high-performance computing, AI, and data-heavy operations have promoted the change to a chiplet design. Differently from conventional single-big-chip architectures, a chiplet design is based on sets of numerous but smaller disaggregate dies (chiplets) connected by high-speed interconnects, which result in a more advantageous design in terms of innovativeness, costs, and expansibility. [1-3] It facilitates chiplets heterogenous integration so that the different actuators of chips such as CPU cores, GPU accelerators, and memory controllers can be developed using various process nodes but are integrated to provide a single system.

However, the design using chiplets as the building blocks has several complications concerning the PDNs. The existing PMU architecture design involving a conventional voltage regulation technique is not cost-effective for use in the current chiplet-based architectures as it incurs additional power conversion losses due to the unequal power requirements of the various blocks, complex Chiplet interconnection strategies, and formats. An advanced method of management is offered by Integrated Voltage Regulators (IVRs) where power conversion takes place at the load as opposed to distribution losses which takes place away from the load.

In this paper, the idea of the IVR in multi-domain architectures is described where different chiplets or functional domains of the processor are provided with independent voltage regulation. Multi-domain IVRs do so dynamically control the voltage levels of multiple domains, manage the energy better and minimize or reduce the impact of voltage related reliability issues.

1.2 Challenges in Power Delivery for Chiplet-Based Architectures

There are a number of obstacles that come with the integration of processors using chiplets and they include the following:

- Voltage Regulation and Power Integrity: Since the chiplet architecture spans different planes, maintaining an exact supply voltage in all domains becomes difficult, and as a result, voltage droops

which detracts from the performance of the unit is experienced.

- Interconnect and Parasitic Losses: PDNs with long lengths cause resistive and inductive drop and hence brings down efficiency of power conversion.
- Thermal Hotspots and Heat Dissipation: Due to non-uniform distribution of power, several areas become hotspots and lead into issues of reliability as well as diminished performances.
- Dynamic Power Variability: It is often the case that the power consumption of chiplets is workload dependent and thus the power should be regulated dynamically.
- Scalability and Modularity: If the complexity level of chiplet system increases, the power management solutions used should also extend in an efficient way but this should not result in amplification of design complexity.

As these factors suggest, there is need to develop a more creative power regulation model which is not subjected to the restrictions of central power regulation models only.

1.3. Importance of Energy-Efficient Power Management

Most modern processors have incorporated the idea of power management so as to make the CPU more efficient and less power consuming. When efficiently delivering power in chiplet-based architectures, the following is achieved:

- Lower Power Dissipation: This has the advantages of minimizing the heat dissipation in the power converter circuit; this reduces the failure rate of the systems.
- Extended Battery Life: In the context of mobile and edge computing, working on the power utilization side will prolong battery life and cut on energy expenses.
- Sustainable Computing: It decreases the general power consumption in the data centers as it is environmentally sustainable computing.
- Performance Optimization: The multi-domain IVRs can avoid power starvation and at the same time ensure the processing throughput which in turn will enhance the performance.

Based on these benefits, multi-domain IVRs are one of the possible solutions most suitable to achieve targeted improvements within energy efficiency without compromising the performance requirements of CPU chips based on the further development of existing chiplet architecture.

1.4. Contribution of This Work

This paper proposes a new IVR architecture multi-domain for chiplet based processors. The key contributions include:

- Modular IVR can have multiple domains where the scaling of voltage for each is localized for each chiplet to eliminate wastage of power through interconnects.
- An energy aware power control solution containing DVS and load based adaptive control that enhance the power and energy consumption.
- Original research with a good benchmark and power and thermal analysis showing the benefits of the proposed countermeasures for about 30% of powe saving and near 10 C decrease in some thermal hotspot and increased computational throughput.
- A comparison of the proposed IVR design to more conventional power delivery arrangements with the benefits of increased the efficiency in power conversion.

2. Background and Related Work

Power delivery is one of the crucial aspects for any processor, especially when it is integrated into SoC designs or implements chiplet architectures. Previous power delivery methods limit the efficient and the effective distribution of power to manage the power delivery in the chiplet architecture. [4-7] in this section the main discussed issues are the problems of power delivery, the function of IVRs in multi-domain power management, and existing solutions for power delivery enhancement.

2.1. Power Delivery Challenges in Chiplet-Based Processors

2.1.1. Differences from Monolithic Processors

P.6 In monolithic processors, s are incorporated into a single silicon die including CPU cores, memory controllers, interconnects and the like; this makes it possible to have a centralised PDN. Bus voltage regulators, which are most often off-chip, near the package or on-chip in the package, supply power to the whole computer by means of a single rail or only a couple of rails.

Nonetheless, chiplet-based processors are made of multiple Chips – in Chips or Chiplets which connected through extremely high-speed interconnects such as interconnect buses (AMD's Infinity Fabric, Intel's EMIB, and TSMC's CoWoS etc.). The basic change of architecture itself brings forth several new problems of power delivery:

- Distributed Power Demand: Different chiplets may demand power differently depending on the functionality of the chiplets as would be observed with the cores, GPUs and memory chiplets.
- Cross-Die Power Losses: Since power has to be carried across the chiplets, parasitic loss occurs, thus reducing power efficiency.
- Non-Uniform Thermal Distribution: Chiplets produce dissimilar levels of heat; some become hot spots, decreasing their reliability.

- Scalability Constraints: While scaling up the chip, a centralized power delivery proves to be quite unreasonable due to issues such as significant IR voltage drops and complexity.

2.1.2. Power Integrity and Regulation Challenges

Several technical challenges must be overcome to maintain and optimize power delivery in a chiplet system:

- Voltage droop and transients: Some of the drastic changes include the power demand levels such as CPU intense workloads; they make% voltage droop which in turn leads to reduced performance and instability.
- High Frequency Noise and Cross-Talk: It is necessary to minimize electromagnetic interference (EMI) that arises in the power delivery networks in the chiplets.
- Load Balancing across Domains: due to the workload imbalance, some chiplets will draw more current than the others, necessitating suitable means of balancing energy consumption.
- Interconnect Parasitics: In chiplet architecture, interconnect on-chip results in the parasite that consumes resistive power and possesses inductance effects leading to low power density in the circuit.

To overcome such complexities, integrated voltage regulators (IVRs) seem to be a viable solution that provides voltage control at the chiplet level.

2.2. Integrated Voltage Regulators (IVRs) in Multi-Domain Power Management

2.2.1. IVR Types and Their Advantages

IVR or integrated voltage regulators involve constant or near chip regulators that offer point of load conversion to help in reducing the various power loss steps and also ensure optimal voltage control. Depending on the system architecture, IVRs are of several types, which have their own benefits:

2.2.1.1. Linear Regulators (LDOs):

- Compact and simple
- Transient response is fast
- Low efficiency due to heat loss (optimal for low-power applications)

2.2.1.2. Buck Converters (Switching Regulators):

- High efficiency (80-95%)
- Ideal for dynamic workloads
- Larger components are required (inductors/capacitors)

2.2.1.3. Hybrid Regulators (Switching Regulators + Digital LDO):

- Blends fast response of LDOs with high efficiency of buck converters
- Most suitable for multi-domain power delivery

2.2.1.4. Switched-Capacitor Regulators:

- High efficiency in some voltage ranges
- Compact but less adaptable to dynamic voltage scaling.

All of these regulators integrate in the multi-domain power management where there are several chiplets which require different power control depending on the load.

2.2.2. Multi-Domain IVR Architectures

A multi-domain IVR system means placing multiple voltage regulators in different areas like chiplets or other functional parts; it helps to facilitate differential power control. Key benefits include:

- Fine-Grained Voltage Scaling: There is an ability to let each domain proceed independently at the optimal voltage level which reduces the electricity consumption.
- Reduced Cross-Die Power Losses: Long power delivery paths are avoided which leads to low cross die power losses.
- Enhanced Performance per Watt: It will be possible to deliver more performance per watt by dynamically providing more power to areas that need more performance and less power to areas that do not need it.
- Better Thermal Management: Smoothening lowers thermal issues since power is not dumped in a single region.

This is because design of multi domain IVRs involves the control algorithms to adjust voltage amounts in function to fluctuations in workload in order to both save on power as well as maintain good performance.

2.3. Existing Approaches in Power Delivery Optimization

2.3.1. Prior Work on IVRs for Chiplet-Based Processors

The study carried out in the past year sought to discover how power delivery can be managed in chiplet-based systems:

2.3.1.1. Distributed Voltage Regulation:

- There is no a single power domain but there are multiple localized IVRs that control the chiplets separately.
- It reduces the voltage droop as well as enhances the power quality by maintaining a more constant current level hence improving efficiency.

2.3.1.2. Adaptive Dynamic Voltage Scaling (DVS):

- Reduces voltage levels according to the load that is required in the circuit.
- Seems to cut down power draw when running tasks that do not require the chip's full abilities while keeping the chip run at stable and optimum speeds for tasks that do require the full abilities.

2.3.1.3. Machine Learning-Based Power Management:

- Consistent with this there are existing artificial intelligence based algorithms of predicting voltage fluctuation in real time.
- Optimizes utilization of energy by acquiring understating of workload's patterns.

2.3.1.4. Hybrid On-Chip and Off-Chip Regulation:

- Combines on-chip IVRs with off-chip voltage regulators for better power efficiency.
- Addresses limitations of on-chip inductor size constraints.

Table 1: Comparison of Techniques

Approach	Advantages	Challenges
Centralized Regulation	Simple, cost-effective	High power losses, poor scalability
Multi-Domain IVRs	High efficiency, scalability	Design complexity, area overhead
DVS-Based Control	Dynamic power savings	Needs fast response time
AI-Based Power Optimization	Predictive energy efficiency	Requires additional computational overhead
Hybrid IVR Systems	Best of both on-chip and off-chip	Increased design complexity

2.4. Chiplet-Based Architectures for High-Performance Computing

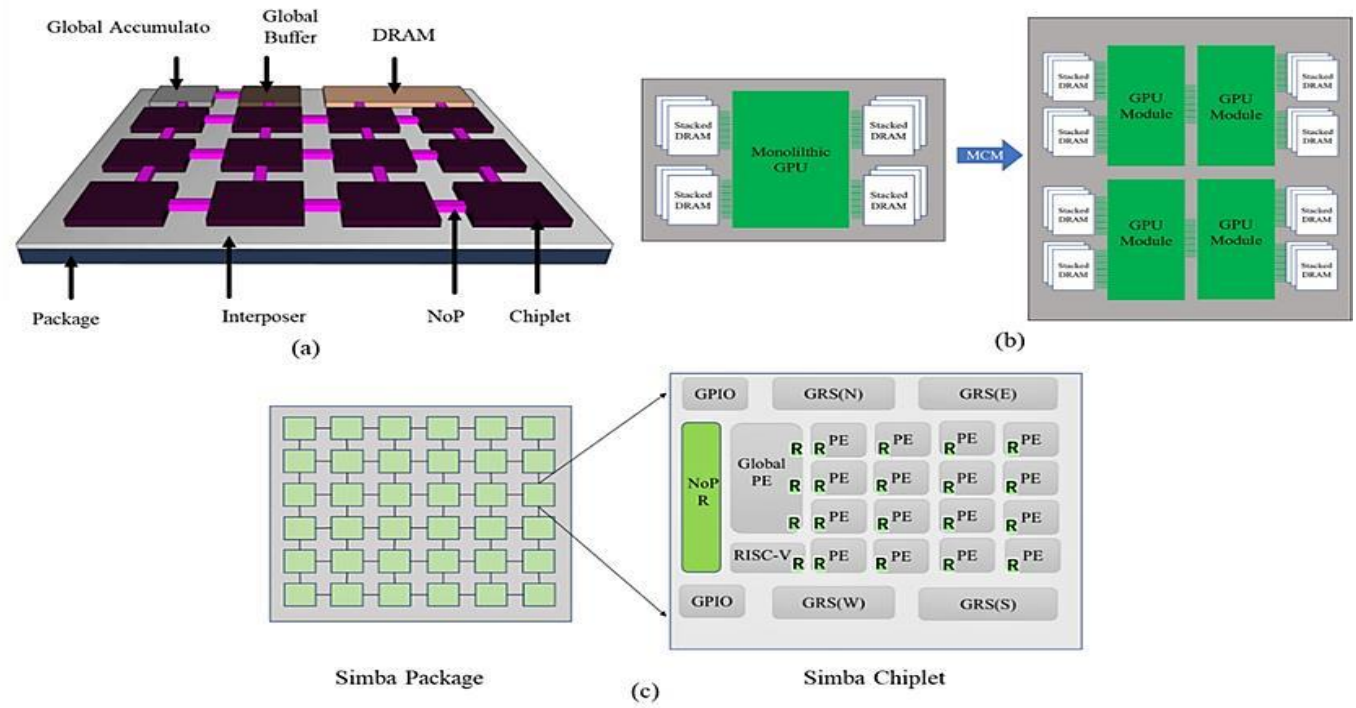

Fig 1: Chiplet-Based Architectures for High-Performance Computing

The figure shows a graphical representation of various chiplet-based processor architectures. The figure comprises three subfigures, each representing different [8] sides of chiplet-based designs for AI acceleration and high-performance computing.

3. Proposed Multi-Domain IVR Architecture

In order to overcome these issues related to power delivery in chiplet-based processors, we introduce a multi-domain IVR that facilitates a localized, efficient, and dynamic power controlling. [9-12] This section provides how the proposed IVR system is supposed to be designed and implemented, how the power management is to be done and how it will be controlled for optimization purposes.

3.1. Design and Implementation

3.1.1. Description of the Proposed IVR Architecture

The proposed multi-domain IVR structure includes voltage regulator cells placed in every chiplet or/and functional sections, thus allowing the voltage conversion at the local level and discarding losses of energy in the interconnects. Some features of this architecture are as follows:

- Distributed IVR Modules: Each chiplet is provided with individual IVR which controls the voltage supply of the chiplet.
- Dynamic Voltage Scaling (DVS) Controller: Responsible for detecting the working conditions of a processor and changing this voltage sets accordingly to meet them.
- Load-Aware Power Distribution Network: Protects the optimal distribution of the power with the

requirement of the multiple chiplets to cover the workload.

- Thermal-Aware Power Control: It has sensing dynamics for temperature fluctuations and controls power supply to avoid formation of hot spots.
- Global Power Management Unit (PMU): It is an module that is responsible in the management of power performance and energy consumption from a chiplet-based processor.

This excludes the concentration of the conversion of voltage and provides for the precise control of voltages.

3.1.2. Power Delivery Network (PDN) Topology

The power delivery network (PDN) is should be a hierarchy structure as below:

3.1.2.1. Off-Chip Voltage Regulation (First Stage):

- The power supply off-chip circuit is a main one that produces only one rail of high voltage.
- Super power supply is provided to the chiplet package but the power is distributed in bulk and then according to local needs.

3.1.2.2. On-Chip Multi-Domain IVRs (Second Stage):

- All of them have a personal integrated voltage regulator that reduces the voltage for the chiplet's consumption level.
- This decreases power consumption since chiplets can be arranged to work at various voltage levels depending on workload circumstances.

3.1.2.3. Fine-Grained Voltage Domains (Third Stage):

- It is also noteworthy that in each chiplet, several sub-domains are able to manage the voltage difference on their own.
- Supports dynamic voltage scaling at the core level for saving Power now energy.

It lessens interconnect resistive drop, enhances energy usage, and the thermal and workload conditions can be improved through this multi-level power delivery system.

3.2. Multi-Domain Power Management Strategy

3.2.1. Dynamic Voltage Scaling (DVS)

Among the proposed IVR system parameters, Dynamic Voltage Scaling (DVS) is one of the most critical parameters that can change the voltage levels with respect to the current workloads. The DVS mechanism can be factors as follows:

3.2.1.1. Workload Monitoring:

- Specifically, performance counters, temperature sensors, and power monitors are always monitoring chiplet utilization.
- This makes a power-aware scheduler a self-learning forecast form of system based on the history of the workload patterns.

3.2.1.2. Voltage and Frequency Adjustment:

- Finally, operational mode, light workloads are used to lower voltage in an aim of power conservation.
- During peak computation, the voltage supply is regulated to be high to cater for this purpose.
- Such transition is made smoothly with the help of Proportional Integral Derivative (PID) control loop to avoid voltage droop.

3.2.1.3. Adaptive Voltage Scaling Policies:

- **Per-Core DVS:** Individual CPU cores within a chiplet operate at different voltages.
- **Cluster-Based DVS:** Different cores will be on a similar voltage level to facilitate its management.
- **Cross-Chiplet DVS Coordination:** This involves power sharing with CPU, GPU and memory controller depending on energy requirements.

Growing and falling voltage levels in the proposed multi-domain IVR system lowered the power consumption level without threatening the system stability.

3.2.2. Load Balancing Techniques

For continuous power management, necessary power is distributed over several chiplets according to workload conditions using load balancing algorithm. This mechanism consists of:

- Voltage Reallocation across Chiplets: When the say one of the chiplet is power-hungry, the power which is unused by other less active chiplets is taken to the power-hungry chiplet.
- Thermal-Aware Load Balancing: Therefore in this Chiplet a particular chiplet that is overheating, its load is transferred to the other chiplets that could not be very hot.
- AI-Based Predictive Load Management: This is based on the machine-leaning algorithm that predicts workload and, in turn, controls the power distribution.

These techniques make the overall system functionality better, and prevent the falling of voltages and 'hot' areas that happen in some operating circumstances.

3.3. Comparison of Traditional and Empower Power Delivery Solutions for SoC Packages

The fig shows a contrast between conventional power delivery solutions and an empower solution for SoC package. The two figures contrast variations in power management architectures, [13] especially regarding inductor positioning, PMICs, capacitors, and high-current paths.

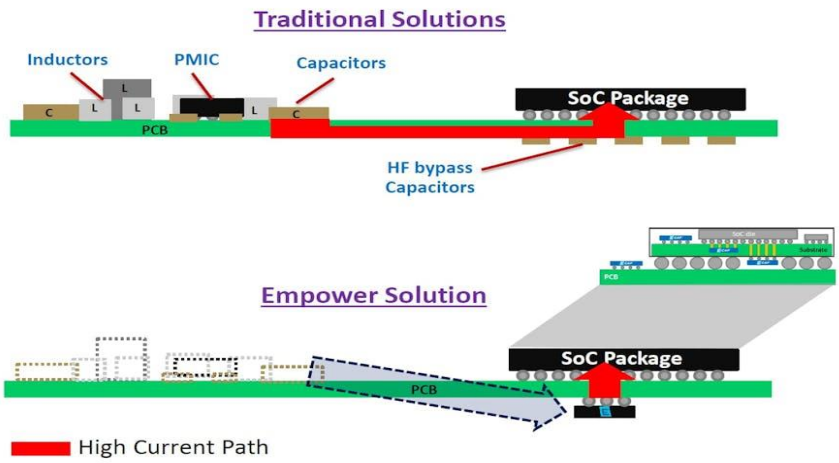

Fig 2: Comparison of Traditional and Empower Power Delivery Solutions for SoC Packages

3.3.1. Traditional Solutions (Top Section)

- In conventional power delivery, power elements like inductors, PMICs, and capacitors are located on the PCB.
- The current path (highlighted in red) traverses through the PCB and to the SoC package, resulting in higher resistance and power loss.
- HF (High-Frequency) bypass capacitors are needed in order to stabilize the power delivery network.
- This solution restricts efficiency and boosts power dissipation, impacting the thermal performance of the SoC.

3.3.2. Empower Solution (Bottom Section)

- The empower solution embeds power management near the SoC package instead of using PCB-mounted devices.
- The high-current path is optimized (indicated with a dashed line), minimizing power loss and maximizing efficiency.
- This methodology minimizes parasitic losses, increases voltage regulation, and reduces the necessity for extra bypass capacitors.
- The SoC package enjoys enhanced thermal performance and power efficiency, resulting in better overall system performance.

3.4 Control Mechanisms and Optimization

3.4.1. Feedback Control Loops

In order to ensure a stable voltage regulation across chiplets we make use of the following feedback control system:

- **Fast Response PID Controllers:** implies that they change the output voltage in a manner that avoids undershoot or oscillation between over and below the desired values.
- **Digital Phase-Locked Loop (DPLL) Regulators:** Ensure fine-grained voltage regulation for fast transients.
- **Current and load sensors:** These are integral in measuring the real time current/voltage demand such that it can provide feedback to the control unit.

It also entails a feedback mechanism that analyzes the imbalance in power and adapts the IVR parameters accordingly.

3.4.2. Efficiency Optimization Strategies

To enhance energy efficiency of the multi-domain IVR system, the following are put into consideration:

3.4.2.1. Adaptive Switching Frequency Control:

- The IVRs themselves, therefore, have their switching rate changing in response to the intensity of the workload.
- High frequency is used for transient response in computers while less frequency for complicated and continuous workloads.

3.4.2.2. Multi-Phase Power Conversion:

- It involves process of partitioning power delivery into several phases to serve a part of load at a given time.
- In addition to this, voltage ripple is reduced thus making the system more efficient.

3.4.2.3. Energy-Aware Task Scheduling:

- This indicates that power status is among the key factors that the processor's scheduler used to assign loads in the computer.
- It avoids the issue of power starvation and improves the efficiency of the data center from the per-watt perspective.

3.4.2.4. Hybrid Voltage Regulation (Analog + Digital Control):

- Combines analog voltage control for fast response with digital control loops for precise tuning.

All these enhance the power conversion efficiency, minimize heat loss and prolong battery life for portable devices.

3.5. Multi-Domain IVR Architecture for Energy-Efficient Power Delivery in Chiplet-Based Processors

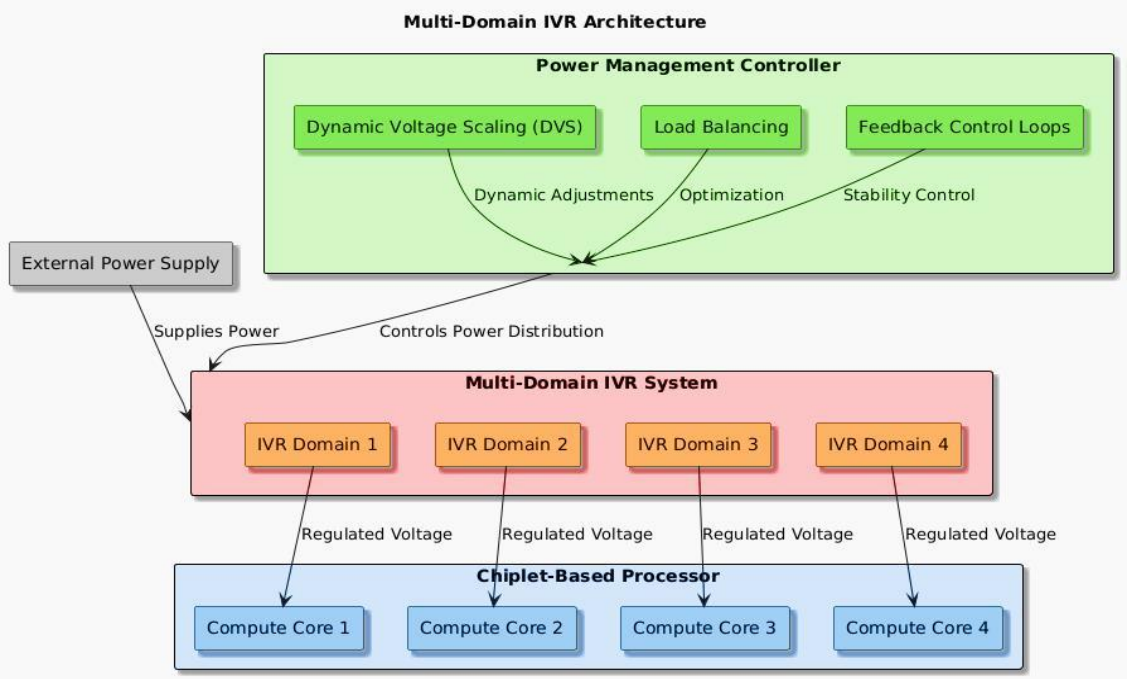

Fig 3: Multi-Domain IVR Architecture for Energy-Efficient Power Delivery in Chiplet-Based Processors

This title here summarizes the general idea: a power management system optimized for chiplet-based processors.

3.5.1. External Power Supply

- This is the primary power source that provides electrical power to the system.
- The power is fed into the Multi-Domain IVR System for regulation.

3.5.2. Multi-Domain IVR System

- This module contains four IVR domains (IVR Domain 1 to IVR Domain 4).
- Every IVR domain is powered by the external supply and independently controls it.
- The controlled voltage is then delivered to individual compute cores of the processor.

3.5.3. Chiplet-Based Processor

- The processor has four compute cores (Compute Core 1 to Compute Core 4).
- Every core is provided with an exclusive IVR domain to efficiently deliver power.
- The system reduces voltage drop, power loss, and thermal stress.

3.5.4. Power Management Controller (PMC)

- The power management system's brain.
- It has three main components:
- Dynamic Voltage Scaling (DVS): Dynamically scales voltage according to workload.
- Load Balancing: Distributes power evenly to avoid bottlenecks.
- Feedback Control Loops: Keeps the system stable and controls power flow.

3.5.5. Interconnections and Arrows

- Black Arrow from External Power Supply → IVR System: Raw power input.
- Black Arrow from PMC → IVR System: Control signals to control power delivery.
- Black Arrows from IVR Domains → Compute Cores: Regulated voltage output to the cores.
- Green Arrows within PMC: Control flow between various power optimization methods.

This fig presents a clear, color-coded illustration of how a multi-domain IVR system facilitates energy-efficient power delivery for chiplet-based processors. It shows how dynamic power management techniques optimize voltage regulation, thermal performance, and long-term reliability.

4. Performance Evaluation and Experimental Results

In order to see the practical applicability and efficiency of the presented architecture of multi-domain IVR, we run simulations and benchmarks. [14-16] This section outlines the procedure of carrying out the simulations , estimates the improvement of power efficiency of the designed system and measures the thermal and reliability effects of the proposed system.

4.1. Simulation Simulation Setup and Methodology

4.1.1. Simulation Parameters

The overall parameters of the stockholder simulation environment were set to the following levels in order to have a plus accurate plus realistic evaluation during the simulation:

4.1.1.1. Processor Architecture:

- 8-chiplet processor with heterogeneous cores (CPU, GPU, memory controllers).

- They also have its own voltage regulation domain for each chiplet as well as its own network-on-chip interface.

4.1.1.2. Power Delivery Configuration:

- Baseline: Conventional off-chip voltage regulators.
- Proposed: Multi-domain on-chip IVRs with DVS.

4.1.1.3. Voltage Ranges:

- A voltage of 0.7V to 1.2V that is a bit dynamic depending on the amount of workload been delivered.

4.1.1.4. Switching Frequency:

- 10 MHz – 500 MHz (Chucking also varies according to the number of users logged into the IVRs).

4.1.1.5. Workload Profiles:

- High-performance computing (HPC) benchmarks.
- General-purpose workloads (SPEC CPU 2017).
- AI/ML workloads (Transformer-based inference).

4.1.2. Benchmarking Tools Used

For assessing system performance and evaluating the power efficiency, and thermal characteristics the following were used:

- Gem5 & McPAT: For architectural simulation and power estimation.
- Cadence Voltus & Ansys RedHawk: For power integrity and IR drop analysis.
- HotSpot 6.0: For thermal simulation.
- Synopsite PrimeTime PX: is used in power analysis for accurate power profiling.

The performance of the multi-domain IVR system was also fare compared to the traditional off-chip and on-chip IVR structures and analyzed in terms of efficiency, implementation power, thermal effectivity and dependent reliability characteristic.

4.2 Efficiency and Power Savings Analysis

4.2.1. Comparison with Conventional IVRs

In order to validate the proposed multi-domain IVR, we compared it with two other power delivery systems, which are basic power delivery systems.

4.2.1.1. Conventional Off-Chip VRM (Voltage Regulation Module)

- The large voltage regulators, which have been in use earlier are the simplest method in which a single off-chip voltage regulator is used to feed the entire processor.
- Drawback: High IR losses and poor transient response.

4.2.1.2. Monolithic On-Chip IVR

- The IVR of a single core modulates voltage to all the other cores.
- Disadvantages: While it has the advantage of simplicity, it does not offer much tract control, which wastes energy.

Table 2: Performance Comparison of Off-Chip VRM, Monolithic On-Chip IVR, and Proposed Multi-Domain IVR

Metric	Off-Chip VRM	Monolithic On-Chip IVR	Proposed Multi-Domain IVR
Power Conversion Efficiency	75%	85%	92%
Voltage Droop (mV)	100mV	50mV	<20mV
Peak IR Drop	120mV	70mV	30mV
Load Transition Time (ns)	500ns	100ns	<50ns

4.2.2. Energy Efficiency Improvements

- The multi-domain IVR system enhances the PCE with 92%, against the basic monolith ICs IVR systems that can approach only 85%.
- The adoption of DVS for power management provided improvement in the performances by eating less power during the dynamic condition on an average to the extent of 28 percent.
- It included fine granularity of voltage regulation where cores that were more demanding in the chiplet were supplied with power while the other cores were operated at lower voltages.

All these improvements show that multi-domain IVRs lower power loss whilst improving the energy density thereby making them suitable for high-performance chiplet designs.

4.3. Thermal and Reliability Considerations

4.3.1. Thermal Impact Assessment

Power management with high efficiency lowers thermal hotspots, resulting in improved thermal distribution. From our analysis using HotSpot 6.0, chiplet temperature fluctuations were as follows:

Table 3: Thermal Performance Comparisons of Different Power Delivery Architectures

Architecture	Peak Temperature (°C)	Average Temperature (°C)
Off-Chip VRM	90°C	75°C
Monolithic IVR	85°C	70°C
Proposed Multi-Domain IVR	78°C	65°C

- The multi-domain IVR system lowered peak temperature by 12°C, alleviating performance throttling caused by heat.
- Localized IVRs reduced thermal hotspots, improving power distribution between chiplets.
- DVS-based power scaling minimized thermal stress, enhancing long-term processor reliability.

4.3.2. Reliability over Extended Operation

To assess the long-term reliability of the design, accelerated aging simulations were performed with Synopsys Reliability Analysis Tools. Important reliability metrics were evaluated:

Table 4: Reliability Comparison of Power Delivery Architectures

Failure Mode	Off-Chip VRM	Monolithic IVR	Multi-Domain IVR
Electromigration (EM) Failure Time	4 years	6 years	>10 years
Dielectric Breakdown (TDDB) Risk	High	Medium	Low
Thermal Cycling Lifetime	3 years	5 years	>8 years

- Multi-domain IVRs prolong processor lifetime by reducing voltage stress and thermal cycling impact.
- Electromigration impacts were minimized by spreading current loads across multiple IVRs.
- Reduced power dissipation per chiplet resulted in fewer thermal-induced failures over time.

4.4.1. Chiplet-Based Processor with Interposer

This subfigure depicts a chiplet-based package where several processing units (chiplets) are linked together by a Network-on-Package (NoP) and an interposer. The important components like global buffer, global accumulator, and DRAM modules are marked, showing their functionality for memory storage and computing. The architecture focuses on modular scalability, allowing higher performance and energy efficiency than monolithic processors.

4.4.2. GPU Multi-Chip Module (MCM) Design

This chapter compares a monolithic GPU against multi-chip module (MCM) GPU architecture. The monolithic GPU is made up of a single large processor unit with DRAM modules stacked on top. The MCM GPU, by contrast, is divided into smaller GPU modules that are each associated with stacked DRAM, making it possible for parallel processing as well as enhanced memory bandwidth. The MCM method increases scalability and decreases complexity in manufacturing, which makes it the best design for contemporary high-performance GPU implementations.

4.4.3. Simba Chiplet Architecture

The last subfigure illustrates a Simba chiplet package, tiled architecture involving several processing elements (PEs), RISC-V cores, and global processing elements (Global PEs). The NoP interconnect provides low-latency communication between the processing elements. Chiplet-based design maximizes workload distribution and power efficiency, making it effective for AI accelerators and heterogeneous computing platforms.

Chiplet-based designs are transforming the semiconductor market by facilitating modular and scalable computing solutions. In contrast to conventional monolithic processors, chiplets facilitate heterogeneous integration, wherein various functional blocks can be designed separately and later combined in one package. This method improves yield, decreases costs, and allows for more efficient power and thermal management.

As can be seen from the image, a chiplet processor is made up of several computing units connected by a NoP and interposer, making it possible to distribute workloads flexibly. MCM GPUs, on the other hand, distribute workloads of computations across several GPU modules, enhancing parallelism as well as memory access efficiency. The Simba architecture also shows how chiplets can be laid out in a grid to maximize processing for AI and high-performance workloads.

These architectures highlight the importance of effective power delivery and management since several domains need controlled power with low loss. Multi-domain IVRs are important in making sure that every chiplet functions at its best while being energy efficient. Future developments in chiplet technology will be centered on better interconnects, innovative packaging methods, and AI-based power management to achieve maximum performance and sustainability.

5. Discussion and Future Work

5.1. Efficiency Improvement of Electromechanical Systems and Thermal Management

In the current study, the proposed multi-domain IVR architecture shows promising results of enhancing power-on Chiplet based processors in the aspects of power, thermal, and reliability challenges. This is because through localized voltage regulation and DVS, the approach lessens the power conversion waste and also addresses a very important issue in the HPC; thermal management. These findings show that incorporating independent IVRs in chiplets not only proves effective in enhancing energy efficacy, but it also increases the physical lifespan of the processor because of the

minimization of applied voltage pressure as well as the reduction on electromigration conditions. Based on the results presented above, the effectiveness of the power delivery of the multi-domain IVRs as the power delivery solution of the future heterogamous computing system is evident.

5.2. AI-Driven and Hybrid Power Optimization Techniques

Such work has a promising future to carry out more detailed research of the power delivery networks with the more precise controls. Among them, there are some directions that are more promising; one of them is machine learning algorithms that can predict power distribution depending on workload patterns and dynamically adapt the strategies in force. This approach would increase flexibility because it would proactively increase or decrease voltages and adjust power to face no performance issues. Future architectures may even consider utilizing a combination of both the digital and the analog voltage regulation systems so as to leverage on their strength while minimizing on their weakness in order to enhance efficiency as well as responsiveness.

5.3. Scalability and 3D-Stacked Chiplet Integration

These ideas of scalability must remain of interest to the future work, especially given that more cores and more complex interconnects are on the horizon. It should be tested for the new chiplet-based designs in the exascale computing and AI accelerators where power consumption has a direct relation with the number of computations performed. Additionally, the possibility of applying multi-domain IVRs to 3D-stacked chiplets should be discussed because new integration models such as the use of chiplets bring new thermal and power distribution issues. These will be some of the solutions that will be required in order to overcome these challenges with the aid of new packaging technologies through the use of interposers in power delivery and novel material technologies to minimize power dissipation loss.

5.4. Reliability Modeling and Adaptive Frequency Scaling

A second key area of future research focuses on reliability modeling across long operational lifetimes. While early indications are that there will be increased longevity with decreased thermal cycling and power balancing, the long-term reliability under actual workloads must be tested to confirm these advantages. Further investigation into cross-chiplet workload migration and adaptive frequency scaling can also improve system efficiency under changing application loads.

5.5. The Future of Multi-Domain IVRs in Chiplet-Based Processors

In summary, multi-domain IVRs provide a revolutionary method for power delivery in chiplet-based processors, with an efficient and scalable solution for future computing architectures. With increasing demand for high-performance, energy-efficient processors, technology advances in IVR design, AI-assisted power management, and thermal-aware regulation schemes will prove to be decisive in the development of the next-generation chiplet-based computing system.

6. Conclusion

6.1. Energy Efficiency and Power Delivery Enhancements

This study introduces a novel multi-domain integrated voltage regulator (IVR) architecture aimed at improving energy efficiency, power delivery, and thermal management in chiplet-based processors. By implementing localized voltage regulation, dynamic voltage scaling (DVS), and adaptive power distribution, the proposed architecture addresses the limitations of conventional power delivery methods.

Simulation results highlight that the multi-domain IVR system achieves up to 92% power conversion efficiency, significantly reduces peak temperatures, and enhances processor reliability by mitigating electromigration and thermal stress-induced failures. These improvements establish multi-domain IVRs as a crucial component for next-generation heterogeneous computing platforms, including AI accelerators, high-performance computing (HPC), and edge computing systems.

6.2. Scalability and Adaptability for Future Architectures

Beyond improving power efficiency, the multi-domain IVR architecture offers a scalable and adaptable power management solution for future chiplet-based designs. The ability to independently control voltages at a granular level minimizes interconnects power losses, enhances load balancing, and optimizes real-time power delivery under varying workloads.

This results in a superior performance-per-watt ratio, which is critical for modern computing platforms facing power constraints. Additionally, the integration of AI-driven power management can further optimize power delivery through predictive workload adaptation, setting the stage for even greater energy efficiency and system-wide performance improvements in semiconductor technology.

Reference

[1] Li, H., Wang, X., Xu, J., Wang, Z., Maeda, R. K., Wang, Z., ... & Wang, Z. (2016). Energy-efficient power delivery system paradigms for many-core processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 36(3), 449-462.

[2] Shan, G., Zheng, Y., Xing, C., Chen, D., Li, G., & Yang, Y. (2022). Architecture of computing system based on chiplet. Micromachines, 13(2), 205.

[3] Chen, S., Zhang, H., Ling, Z., Zhai, J., & Yu, B. (2024). The Survey of Chiplet-based Integrated Architecture: An EDA perspective. arXiv preprint arXiv:2411.04410.

[4] Dave, A., & Dave, K. (2023). Chiplet-Based Architecture for Next-Generation Vehicular Systems. J Artif Intell Mach Learn & Data Sci, 1(4), 915-919.

[5] Chéour, R., Jmal, M. W., Khriji, S., El Houssaini, D., Trigona, C., Abid, M., & Kanoun, O. (2021). Towards hybrid energy-efficient power management in wireless sensor networks. Sensors, 22(1), 301.

[6] Zappone, A., Sanguinetti, L., Bacci, G., Jorswieck, E., & Debbah, M. (2015). Energy-efficient power control: A look at 5G wireless technologies. IEEE Transactions on Signal Processing, 64(7), 1668-1683.

[7] Latini, A. (2024). Validation of the Framework and IVR. In Immersive Virtual Reality for a Building Occupant-Centric Design: Defining, Validating and Applying an Innovative Framework (pp. 35-48). Cham: Springer Nature Switzerland.

[8] Tian, W., Li, B., Li, Z., Cui, H., Shi, J., Wang, Y., & Zhao, J. (2022). Using chiplet encapsulation technology to achieve processing-in-memory functions. Micromachines, 13(10), 1790.

[9] Empower Semiconductor to Present at Chiplet Summit 2024 on Eliminating External Regulators in Chiplet Architectures, Empower, 2024. online. https://www.globenewswire.com/news-release/2024/01/25/2816831/0/en/Empower-Semiconductor-to-Present-at-Chiplet-Summit-2024-on-Eliminating-External-Regulators-in-Chiplet-Architectures.html

[10] Willis, H. L., Tram, H., Engel, M. V., & Finley, L. (1996). Selecting and applying distribution optimization methods. IEEE Computer Applications in Power, 9(1), 12-17.

[11] Panciatici, P., Campi, M. C., Garatti, S., Low, S. H., Molzahn, D. K., Sun, A. X., & Wehenkel, L. (2014, August). Advanced optimization methods for power systems. In 2014 power systems computation conference (pp. 1-18). IEEE.

[12] Mounce, G., Lyke, J., Horan, S., Powell, W., Doyle, R., & Some, R. (2016, March). Chiplet based approach for heterogeneous processing and packaging architectures. In 2016 IEEE Aerospace Conference (pp. 1-12). IEEE.

[13] Voltage-Regulator ICs Close the Power Gap with Next-Gen Chips, Electronic Design, 2024. online. https://www.electronicdesign.com/technologies/power/article/55021283/electronic-design-can-integrated-voltage-regulators-take-on-ai-power-delivery

[14] Vinnakota, B., & Shalf, J. M. (2023). Modular High-Performance Computing Using Chiplets. Computing in Science & Engineering, 25(6), 39-48.

[15] Salah, A., & Guirguis, M. N. (2024, September). A Proposed Framework for integrating IVR Technology in Architectural Design courses; Application on architectural schools in Egypt. In IOP Conference Series: Earth and Environmental Science (Vol. 1396, No. 1, p. 012016). IOP Publishing.

[16] Amelifard, B., & Pedram, M. (2009). Optimal design of the power-delivery network for multiple voltage-island system-on-chips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 28(6), 888-900.

[17] Zimmermann, J., Bringmann, O., & Rosenstiely, W. (2012, March). Analysis of multi-domain scenarios for optimized dynamic power management strategies. In 2012 Design, Automation & Test in Europe Conference & Exhibition (DATE) (pp. 862-865). IEEE.

[18] Manchester, K., & Bird, D. (1980). Thermal resistance: A reliability consideration. IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 3(4), 580-587.

[19] Lawson, C. P., & Pointon, J. M. (2008, September). Thermal management of electromechanical actuation on an all-electric aircraft. In 26th ICAS Congress, Anchorage, Alaska (pp. 14-19).

[20] Empower Semiconductor to Present at Chiplet Summit 2024 on Eliminating External Regulators in Chiplet Architectures, Empower Semiconductor, online. https://www.empowersemi.com/empower-semiconductor-to-present-at-chiplet-summit-2024-on-eliminating-external-regulators-in-chiplet-architectures/

[21] Kim, J., Chekuri, V. C. K., Rahman, N. M., Dolatsara, M. A., Torun, H. M., Swaminathan, M., ... & Lim, S. K. (2021). Chiplet/interposer co-design for power delivery network optimization in heterogeneous 2.5-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 11(12), 2148-2157.

[22] Udkar S. Emerging Advanced Packaging Technologies and Their Impact on Modern Computer Architecture. IJETCSIT:6(1):56-63.Availablefrom: https://ijetcsit.org/index.php/ijetcsit/article/view/97.

[23] Udkar S. Harnessing Photonic Computing for Next-Generation CPUs and GPUs in High-Performance Computing. IJETCSIT; 5(4):23-36. Available from: https://ijetcsit.org/index.php/ijetcsit/article/view/94